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Electronic calibration developed for the CMS electromagnetic calorimeter

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Abstract

An electronic system, designed to provide a relative calibration for the readout of the CMS electromagnetic calorimeter (CMS-ECAL), is described. On request, this system injects a pulse at the input of a predetermined group of preamplifiers with preselected amplitude and a shape identical to the one produced by the photodetectors. Several chips, in DMILL 0.8 μm technology, have been developed for integration on the front-end electronics. We describe the principle, the testing, the measurement of their precision, and radiation hardness.

1. Introduction

The electromagnetic calorimeter (ECAL) is an essential part of the CMS experiment. It has been designed to measure the energy of electromagnetic particles in a range from 50 MeV to 2.5 TeV with the extremely ambitious challenge of a stochastic term = 2%, a calibration term = 0.5%, and a noise term = 150 MeV [1].

This exceptional resolution is specifically needed between 20 GeV and 300 GeV to extract from background the electromagnetic decay of the Higgs boson, if its mass is in the range 100–200 GeV. Under 20 GeV, the resolution is less important since the tracking device is more precise than the ECAL. Above 300 GeV, the products of new physics phenomena can be observed even with a resolution of the order of 1% (dominated in this region by the calibration).

A calibration with a precision of 0.5% on a 10^5 -channel detector has never been achieved so far and certainly requires several redundant methods of evaluation. Our electronic calibration has been designed to contribute to this challenge, with different aims, according to the phase of the experiment. During the mounting and maintenance periods, it will help us to understand and debug the detector; during data-taking periods it will provide the specific calibration parameters of the readout electronics.

2. Calibrations for the ECAL detector

In our project, the calibration of the CMS-ECAL is based on several partially redundant methods:

1. Light calibration: Light pulses, produced by two central lasers, are dispatched through optical fibres and injected into each crystal at its inner face. The wavelength of the main laser has been chosen in the middle of the scintillation spectrum of PbWO_4 (420 nm) in order to measure the loss of transparency of the crystals under irradiation at this wavelength [2,3]. The wavelength (600 nm) of the second laser has been chosen in the region where the transparency of the crystals is mainly insensitive to radiation ageing; it is foreseen to follow the drifts of the overall readout (APD and electronic).
2. Electronic calibration: A charge is injected at the input of the readout chain to cross-calibrate the multigain preamplifiers and calibrate the digitization.
3. Inter-calibration: At low energy, the isolated electrons are measured precisely by the tracker and their momentum is compared with the response of the calorimeter.

1 : Lapp, Annecy-le-Vieux, France.

2: CERN, Geneva, Switzerland.

4. Absolute calibration with physics events: At medium energy (up to ~ 100 GeV), the abundant yield of W's and Z's will provide an absolute calibration for the whole calorimeter. Depending on the luminosity, this ultimate calibration process will need between a few days and a month, during which the different relative calibrations of the different regions of the detector will have to be anchored.

3. The ECAL readout chain

The overall readout electronics was described at the start of the project. It is still under development and may change again.

3.1. Principle

A pair of twinned APDs, stuck on the back face of every crystal, produces an electronic pulse (1 ns rise time and 15 ns fall time) with an integrated charge of ~ 100 electrons/MeV. These photodetectors are connected to a multigain, floating point preamplifier (FPPA), which transforms the APD pulse into a smoother one (40 ns rise time and 60 ns fall time), which is sampled at 40 MHz. For each sampling, the system selects among the four amplifiers of the unit, the one that has the highest gain and is not saturated (later named 'best amplifier'), and sends the amplified sampling to a 40 MHz flash ADC. A 'word builder' concatenates the 12 bits produced by the ADC with the 2 bits indicating the selected amplifier. Every 25 ns, for every channel of the detector, these 14 bits are transferred to the control room, through optical fibres, 80 m long, clocking at 1 GHz.

3.2. The readout front-end card

Every front-end board reads five channels. It contains a control chip (CTRL) that recognizes and dispatches the ingoing and outgoing information, five FPPAs, five ADCs and one serializer–deserializer connected to an optotransmitter (Fig. 1). Apart from supplies and grounding, every board is connected to the outside world through optical fibres only.

According to a code given to the CTRL, the same readout chain can be asked to read either the APD signal (data mode), or the temperature (from probes installed on the crystals and APDs), or the dark current of every APD.

3.3. The readout chips

- 1) The CTRL: The control chip is the local manager. It receives orders from the control room through optical links; it decodes and dispatches them to the different chips of the readout board, determines the measurement mode (data, temperature or dark current), organizes the electronic calibration (amplitude of the pulse and trigger), fixes the FPPA thresholds, adjusts the relative delays between channels etc.
- 2) The FPPA is a four-gain preamplifier system; it was developed at IPN (Lyon, France) and CERN, in the UHF1X Harris process. It receives input signals from the APDs and from the temperature sensors by a short (10 cm) Kapton flat cable. Every 25 ns, it generates an analog signal corresponding to the sampled amplitude multiplied by the best gain and at the same time, on its digital output a 2-bit word, flagging the amplifier that has been used. The electronic gain is then optimized for every sampling of every pulse. The amplitudes at which the gains are shifted are individually adjusted by thresholds, which can be fine-tuned by internal DACs.
- 3) The sampling ADC: Every sampling is kept in a sample and hold circuit and sent to a 40 MHz 12-bit commercial sampling ADC: AD9042 from Analog Device.

This was chosen for its intrinsic performance and its radiation-hardness capabilities.

- 4) The optical link: the outgoing information passes through a gigahertz serializer followed by a light emitter and the ingoing information passes through a receiver and a deserializer. This system was developed in ASGA technology to optimize its overall power consumption, reduced to 30 mW.

As mentioned in the introduction, all these chips are still under development.

4. Electronic calibration

4.1. Description

4.1.1. The system

The technical choices were driven by pragmatic requirements:

1. The calibration management orders must use the same structure as the readout management ones.
2. The power consumption has to be minimized and should use the existing supplies (0/5 V).
3. The readout chain characteristics must not be deteriorated, in particular no addition of cross talk or noise (specifically correlated noise). The pulse generators have to be implemented in or close to the FPPAs to avoid noise and cross talk.
4. The calibration has to be at least as precise and reliable as the readout chain (in particular in terms of irradiation hardness).
5. The segmentation has to be as fine as possible: the lowest level for calibration addressing (amplitude and trigger) has to be the front-end card.

The electronic calibration system is mainly based on three chips:

1. The Test Pulse Logical System (TPLS) is integrated in the CTRL: from the overall traffic, it selects, decodes, and dispatches the information relevant for electronic calibration.
2. The DAC builds the common amplitude level for the five injectors of the same board.
3. The injector (one per FPPA) generates, when triggered, a pulse of current on the input of the preamplifier.

4.1.2. The Test Pulse Logical System (TPLS)

The TPLS is in charge of the selection of the calibration information, the decoding, the loading of the digital word in the calibration DAC, and the building of a trigger window (400 ns) for the pulse injector.

The calibration protocol information is foreseen to fit inside the general protocol of data exchange between the control room and the front-end boards. The basic elements for this protocol are groups of 8-bit frames, transmitted at 40 MHz. The first four bits of every frame are dedicated to the readout organization and the last four bits to calibration. A calibration trigger is made in three steps:

- a) a 12-bit word is built by merging three successive frames and then transferred to the DAC,
- b) the DAC is loaded,
- c) the trigger window is built, and sent to the injector.

The sequence of frames for a calibration trigger is then [TV-TV-T1-T2-TV-T3-T4-TV-T5-T6-TV-T7-T8], where TV are empty frames, T1 to T5 build the amplitude word, T6 loads the DAC, and T7 to T8 trigger the injector.

4.1.3. The DAC

We have chosen a commercial 12-bit DAC in CBCMOS technology: the AD8582AR, (from Analog Device), for its characteristics, well adapted to our needs. Supply: 0/5 V;

power dissipation when unloaded: 20 mW; range: 0-4 V; resolution: 1 mV; max current on output: 5 mA.

A dedicated output pin allows the measurement of the reference produced by the band-gap. This commercial chip has radiation hardness capabilities that we have checked.

4.1.4. The Analog injector

The analog injector is the most critical part of this system. The calibration process starts by installing an amplitude level produced by the AD8582AR and then, a series of 400 ns negative trigger windows. At the falling edge of every window, this system injects a current pulse, with a fast negative fall edge (<1 ns) followed by an exponential rise ($\tau = 15$ ns) to the preamplifier input; 400 ns later the rising edge of the window generates an unused positive pulse. We have checked that this unused positive pulse does not perturb or deteriorate the preamplifiers.

The electronic characteristics of this device have been adjusted to the physics requirements: a total dynamic range equivalent to that of the detector (peak current of 4 mA, and a total charge of 48 pC), a dispersion to linearity better than 0.5%, a stability in the pulse shape better than 1%, and an extremely low Power Supply Rejection Ratio (PSRR) on both the supply and the DAC lines. Its radiation hardness has to be safe up to at least 10^{14} n/cm² and 3 Mrad in γ (equivalent to 10 years of LHC running conditions).

Using the multiproject processes facility, we have made five generations of prototypes; a first one in AMS technology to test the principle, three versions in CMOS technology, and one version to test the integration of the five channels in one chip.

In the final design, the injector is made of three parts (Fig. 2):

1. The receiver adapts the level of the PECL trigger window produced by the TPLS and sharpens its edges in order to avoid the dispersion in time definition.
2. The trans-impedance amplifier translates the voltage level produced by the DAC into a current level, needed by the pulse generator.
3. The pulse generator is mainly a two-branch bipolar circuit. When triggered, it tips the flowing current from one branch to the other. The capacitance C_{out} (60 pF), rapidly discharges and then recharges through R_{out} (250 Ω). The decay time of the pulse is then ($R_{out} \times C_{out}$). In order to fix the decay time whatever the process dispersions on R_{out} , the capacitances C_{out} were placed outside the chip as CMS components, to allow an individual, precise adjustment of the product ($R_{out} \times C_{out}$).

The overall power consumption of this injector, one of our major concerns, was reduced to 20 mW for $V_{DAC} = 0$, up to a maximum of 55 mW for $V_{DAC} = 1$ V. This power dissipation varies by 2.3% according to the process dispersions and by 2.9% for a temperature increase from 27°C to 70°C.

The other dispersions have been systematically evaluated both by simulation and by measurements.

a- Dispersions due to the foundry process ('worst case simulation'): We found no measurable variation in the slope Q_{out}/V_{DAC} , slight dispersions of 5 mV on the threshold (defined as the value of DAC at which the injector signal starts to increase), slight dispersions on the linearity (0.25% at 10 GeV) and on the saturation level (1.3%).

b- Temperature: When the temperature varies from 27°C to 70°C, the only measurable effect is a slight drift of the thresholds from 35.7 mV to 33.7 mV.

In order to fulfil the required precision, the chips will have to be individually pre-calibrated on the final boards and the offset (Q_{out} for $V_{DAC} = 0$) will have to be remeasured periodically during data taking.

4.2. Qualification of the prototypes

4.2.1. Qualification procedure

Figure 3 shows the chain that has been mounted to qualify the different components of the project. This chain is essentially composed of a PC monitoring a VME crate and a CAMAC crate. These crates contain different sampling and charge ADCs and custom modules to simulate specific CMS protocols controlling the system. A precise multimeter (for voltage measurements) and a digital oscilloscope (to measure the shape of the injector pulse), both linked to the PC by GPIB, have also been used.

According to the type of measurement, the same program can test either the transmission and decoding capabilities of the TPLS with statistic on eventual errors, or the precision of the DAC, or the precision in linearity of the injector, or the effects of radiation on the response of the different parts of the system.

A linearity measurement run consists of building a ramp of increasing amplitude on the DAC and measuring the answer of the injector, through a high-quality amplifier. For every step of ramping, the PC computes the average response and the root mean square over 10 triggers on the ADCs, or the voltage response on the multimeter. When the ramping is finished, a linear fit is performed on the straight part of the line; a chi square and a residues distribution are then computed.

4.2.2. Qualification measurements

a) Qualification of the TPLS

Extensive tests were carried out both in transmission and decoding; the default rate was found to be lower than one part per million, even under and after irradiation.

b) Qualification of the AD8582A

The qualification of the DAC consisted in the measurement of the offset (output voltage for DAC = 0), and the evaluation of the slope (mV/bit), of the fitted offset and of the residues to a linear fit on the linear part of the response.

Table 1 and Fig. 4 show the dispersion in linearity and the residues (in millivolts and in per cent) to a linear fit (1 LSB = 1 mV).

It can be seen that the deviations from linearity are always better than 0.3 LSB.

c) Qualification of the injectors

For every injector prototype foundry, we measured on at least five chips:

1. the measured offset (charge response of the injector for DAC = 0),
2. the threshold (DAC value at which the injector starts to increase),
3. the parameters of the linearity (slope, threshold, residues etc.),
4. the saturation voltage (highest input voltage for which the distance to the fitted line starts to be larger than 1%),
5. the dynamic range (defined as the range between threshold and saturation, where the linearity residues become systematically larger than 1%).

The linearity of the injectors was measured either by the voltage drop at the edges of R_{out} (which is more precise than the charge measurement), or by the integrated charge

with a precise 13-bit ADC. In some runs, we also verified on the digital scope that the shape of the pulse did not change with amplitude, irradiation, temperature, etc.

4.2.3. The linearity

The linearity of the injector is a convolution of the linearity of the trans-impedance amplifier by the linearity of the pulse generator. Our chip prototypes were designed to allow the evaluation of both contributions.

a- Linearity of the transimpedance amplifier

Table 2 and Fig. 6 show the dispersion of the linear parameters and the residues on the linear fit to the response of the AMS prototype amplifiers.

b- Global linearity of the injector

Figures 5 and 6 and Tables 2 and 3 show an example of the residues to the linear fit both in charge and in voltage (as described in Section 4.2.2. c). These measurements were made on the two first generations of prototypes in the AMS and DMILL technologies. It shows significant dispersions at low amplitude which have been correlated to the technological dispersions between different foundries. In DMILL, for a given wafer, the corresponding dispersions between the centre and the edges are of the order of 2-5%.

4.2.4. PSSR measurements on the injector

We measured the transfer ratio between the supply or the DAC inputs and the injector output with a spectrum analyser connected on the pins of the chip. Figures 7 and 8 show the rejection ratio in both the inactive and active modes of the injector on +5 and -5 supply lines and on the DAC line. Between 10^3 and 10^8 Hz, the ratio is better than 60 dB for supplies and 80 dB for the DAC, with a difference of 20 dB between the active and the inactive injector mode. This noise is always = 0.5 nV/vHz.

5. Irradiation tests

During 10 years of LHC running, we expect an integrated luminosity of $5 \times 10^5 \text{ pb}^{-1}$. During this period, the readout electronics of the CMS ECAL will integrate a dose of the order of 10^{13} neutrons/cm² and 300 krad of gammas in the barrel and 10^{14} neutrons/cm² and 1 Mrad in the end caps. We have tested the hardness of our prototypes for such doses under both neutron and gamma irradiations.

5.1 Irradiation sources

- a) Neutron sources: After a preliminary test on the Ulysses nuclear plant at Saclay (Run 1), we used the SARA cyclotron installation in Grenoble (France) (Run 2, up to 1.5×10^{13} n/cm²) and after its definitive shutdown, the CERI installation in Orléans (France), where the neutron beam irradiation facility had been moved (Run 3, up to 6.5×10^{13} n/cm²; Run 4 up to 10^{14} n/cm² and Run 5 up to 1.1×10^{15} n/cm²). The SARA and CERI beams [4, 5, 6] produce neutrons by stripping off deuterons from a thick beryllium target. The average energy of these neutrons is ~ 6 MeV with a FWHM of ~ 6 MeV. The fluency can be adjusted by the distance to the target, with a maximum of 10^{13} n/cm²/hour. The photon contamination to these neutron beams has been evaluated at 3.6 kGy for an integrated dose of 2×10^{14} n/cm². The absolute normalization of the integrated doses was obtained by measuring the irradiation of small nickel washers, stuck on the chips and analysed later at ISN (Grenoble).

- b) Gamma source: We irradiated an injector designed for the barrel up to 400 krad, (Run 8) on a cobalt source facility at PSI (Villigen). During this test, owing to safety requirements, the chip was not powered.

5.2 Results on neutron irradiation

In order to measure online the eventual degradation of the tested chip, the boards containing the chip were linked either to the control room or to other specific boards, deported far enough from the neutron beam. Figure 9 shows the set-up that we used.

1. TPLS: We irradiated the TPLS in neutron beams during Runs 3 and 4 and found neither deterioration nor single electron error induced by irradiation up to $11.5 \times 10^{13} \text{ n/cm}^2$ and 36 Mrad.
2. DACs: The DAC is mainly made of three parts: *i)* a band gap that produces a voltage reference stabilized against supply and temperature drifts; *ii)* a divider that organizes the steps; and *iii)* an output buffer that allows the DAC to drive the output current.

Figure 10 shows the drift of the voltage reference under neutron irradiation (which measures the band gap hardness) for two different DACs. The V_{ref} shift is $< 0.2\%$ for an equivalent integrated dose of 10 LHC years. For the output voltage of the DAC, this produces no shift on the offset and a slope variation of 0.2% .

We tested the linearity of the DAC under neutron irradiation up to $6 \times 10^{13} \text{ n/cm}^2$. We found a drift of -0.5% on the reference voltage, 2 mV on the offset and -0.6% on the slope. We saw no effect on the divider part of the DAC.

3. The injectors: The injectors were irradiated in all the neutron sources previously mentioned. We evaluated the drifts in measured offsets, and in linearity (fitted offset, slope and range).

For an integrated dose of $2.9 \times 10^{13} \text{ n/cm}^2$, the main average changes are 0.7% on the slope and 3 mV on the offset. Figure 11 shows an example of these measured irradiation effects.

Run 5 was a test to evaluate the hardness limit of our injectors under irradiation. We submitted them to an integrated dose of $1.1 \times 10^{15} \text{ n/cm}^2$ (and 400 krad of gammas). Figure 12 shows the variation in slope ($\sim 1\%$). Figure 13 shows the main effect: a drastic reduction of the dynamic range by a factor 3 due to a drop of the saturation voltage. Later on, in the laboratory, this effect was recovered up to 96% by heating the chip at 80°C for three days.

6. Application of the electronic calibration on beam measurements

This electronic calibration was mounted on a specific set-up dedicated to the precise evaluation of the ageing of the CMS crystals under irradiation on a test beam at CERN (GIF facility). For this evaluation, we alternated runs during which a group of crystals are irradiated by a Cs137 source under 15 rad/hour, and runs during which their response to an electron beam is precisely measured. A sophisticated calibration by light injection from a laser and from LEDs is used to follow the transparency variation due to irradiation. Figure 14 show an example of corrections that are applied off-line to correct the readout drifts during a stabilization run (without irradiation), for LED data.

Figure 15 shows that when the readout is stable, the calibration does not deteriorate the data.

7. Conclusions

We designed an electronic calibration system for the CMS-ECAL readout chain. Several analog and logic chips were founded in the DMILL process and tested. We proved that this system is stable in real experimental conditions and resistant to noise injected on any connections and to irradiation damage up to 1.1×10^{15} neutrons/cm² (3.6 Mrad).

This set-up, designed for the next generation of LHC experiments, can be adapted to any detector readout chain, working in a hostile environment in terms of temperature, radiation rate, inaccessibility, needing extreme reliability, low power consumption, etc.

For complex, high-granularity detectors, this tool is well adapted to understanding and debugging the cabling during installation and interventions, to understanding breakdowns, and during data-taking to intercalibrating the different channels or different regions of the detector. It clearly has to be integrated from the beginning in the electronic readout design, as a major component of the readout.

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Figures and Tables

Figure 1: Principle of the ECAL readout

Figure 2: Principle of the injector

Figure 3: Principle of the electronic set-up for chip measurements

Figure 4: Residues (in mV and %) to linear fit on AD 8582

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Figure 6: Residues in Q_{out} and V_{out} on linear fits, for six different DMILL bipolar injectors

Figure 7: Power supply rejection ratios (PSRR) on the -5 V (top) and $+5$ V (bottom) lines of a DMILL BiCMOS injector

Figure 8: PSRR on the DAC line of a DMILL BiCMOS injector

Figure 9: Set-up for measurements on neutron beam

Figure 10: Drift of the V_{ref} for two DACs under irradiation

Figure 11: Examples of variations of the fitted offset and slope under irradiation

Figure 12: Shift of the slope and the offset for extreme irradiation

Figure 13: Variation of saturation under irradiation

Figure 14: Example of correction by electronic calibration of a readout drift

Figure 15: Example of correction applied on a LED signal without and with TP corrections (the data are not deteriorated by corrections)

Table 1 : Dispersion in DAC linearity as measured in the laboratory

Table 2 : Results of linear fit on the input amplifier of the AMS injectors

Table 3 : Technological dispersion in charge linearity for the DMILL injector chips

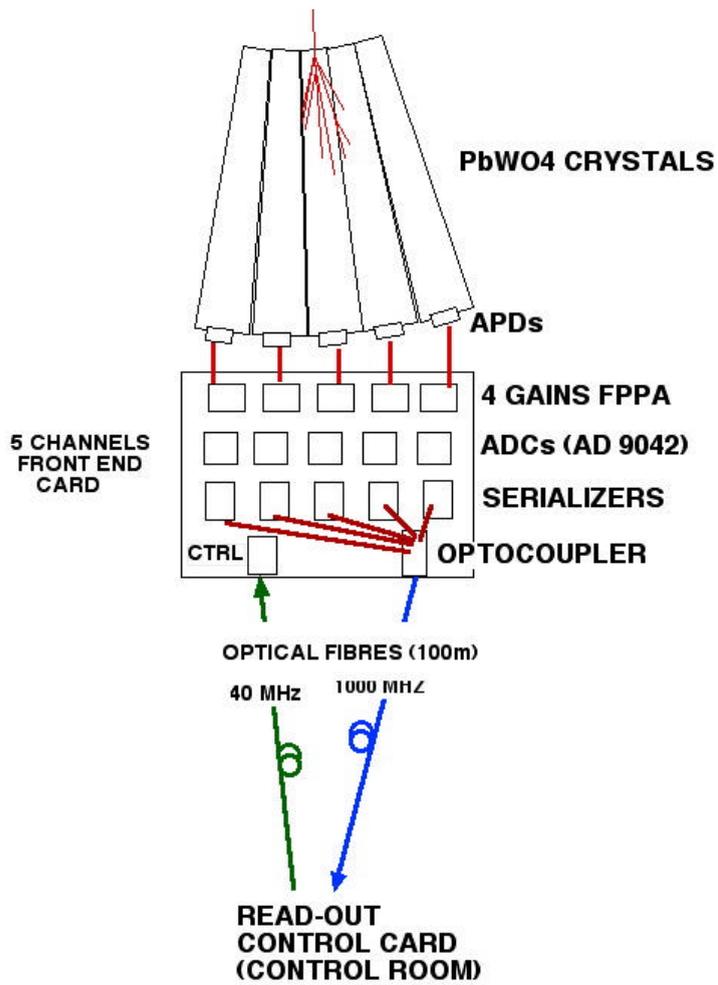


Figure 1: Principle of the ECAL readout

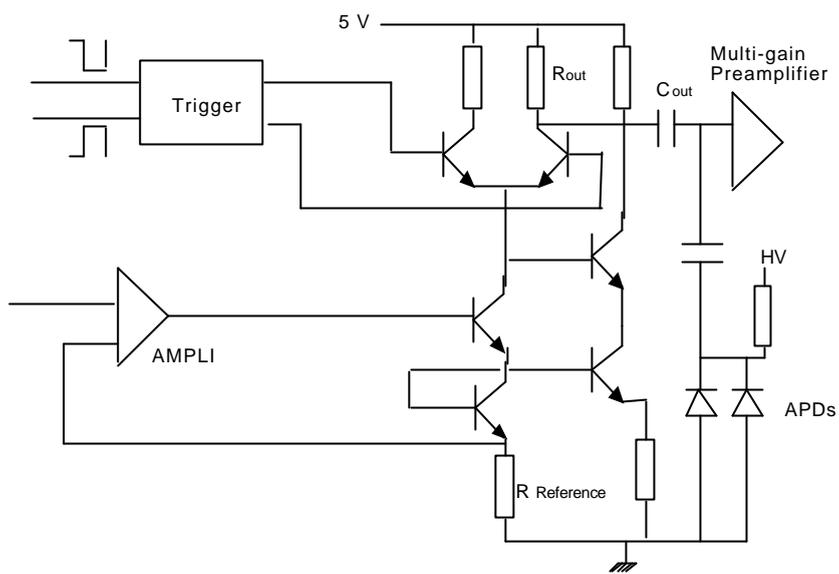


Figure 2: Principle of the injector

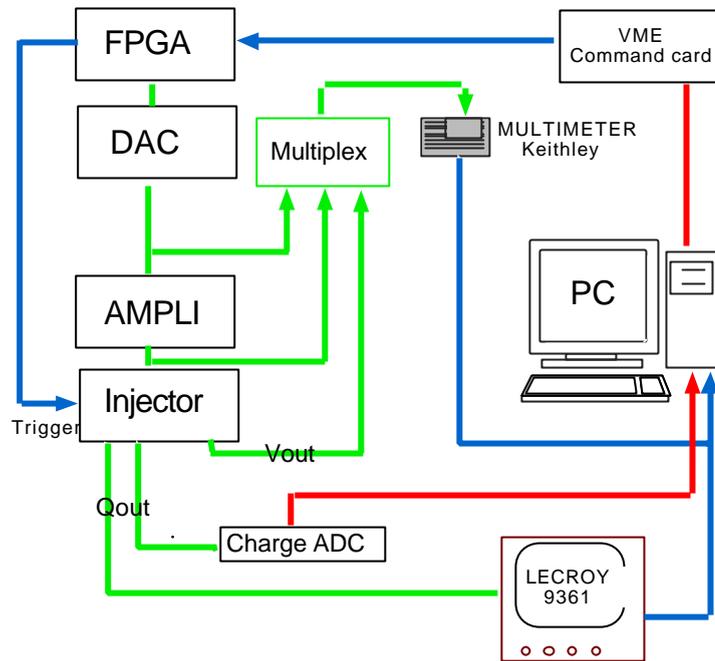


Figure 3: Principle of the electronic set up for chip measurements

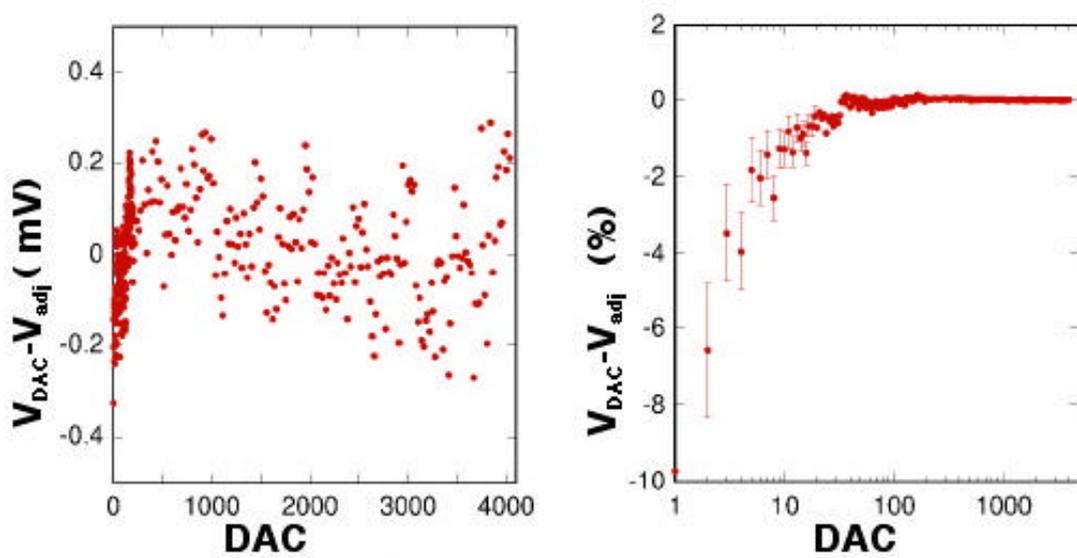


Figure 4: Pools (in mV and %) to linear fit on AD 8582

Table 1: Dispersion in DAC linearity as measured in laboratory

| DAC | Adjusted slope | Adjusted offset(V) | Measured offset (V) |
|---------|----------------|--------------------|---------------------|
| 1 | 0.99947 | 0.0010658 | 0.0007449 |
| 2 | 0.9998 | 0.0009184 | 0.0006529 |
| 3 | 1.0012 | 0.0009744 | 0.0006780 |
| 4 | 1.0009 | 0.0007302 | 0.0004752 |
| 5 | 0.9996 | 0.0009378 | 0.0006508 |
| 6 | 0.99968 | 0.0009172 | 0.0006571 |
| Average | 1.001 ~ 0.9995 | 0.0007 ~ 0.001 | 0.0005~0.0008 |

Table 2: Results of linear fit on the input amplifier of AMS injectors

| Injector | Slope | Adjusted offset (V) | Measured offset (V) | Saturation (V) |
|----------|---------------|---------------------|---------------------|----------------|
| 1 | 1.0005 | -0.003257 | 0.0043 | 1.497 |
| 2 | 1.0000 | -0.0030909 | 0.0045 | 1.494 |
| 3 | 0.99967 | -0.00107 | 0.0044 | 1.501 |
| 4 | 1.0006 | -0.001501 | 0.0043 | 1.503 |
| 5 | 1.0003 | -0.0032399 | 0.0043 | 1.503 |
| Average | 1.0006/0.9996 | -0.004/-0.001 | 0.0043/0.0045 | > 1.494 |

Table 3: Technological dispersion in charge linearity for DMILL injector chips

| Injector | Slope | Adjusted offset (pedestal incl.) | Saturation (pedestal incl.) | Dynamic range (ch.) |
|----------|--------|----------------------------------|-----------------------------|---------------------|
| 1 | 2401.7 | 864.92 | 4497 | 3632 |
| 2 | 2425.1 | 863.06 | 4511 | 3648 |
| 3 | 2393.8 | 864.41 | 4468 | 3604 |
| 4 | 2413.2 | 866.12 | 4498 | 3632 |
| 5 | 2379.5 | 863.29 | 4446 | 3583 |

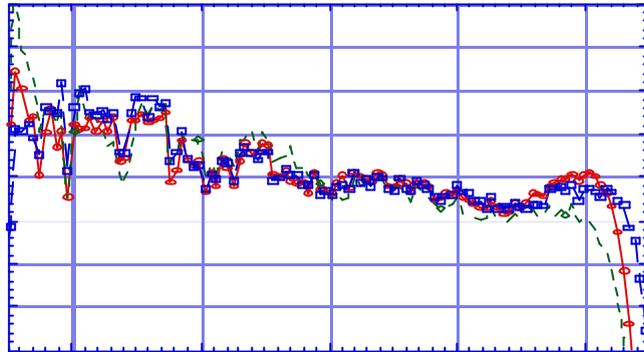


Figure 5: Pools of the fit (%) on the input amplifier of AMS injectors

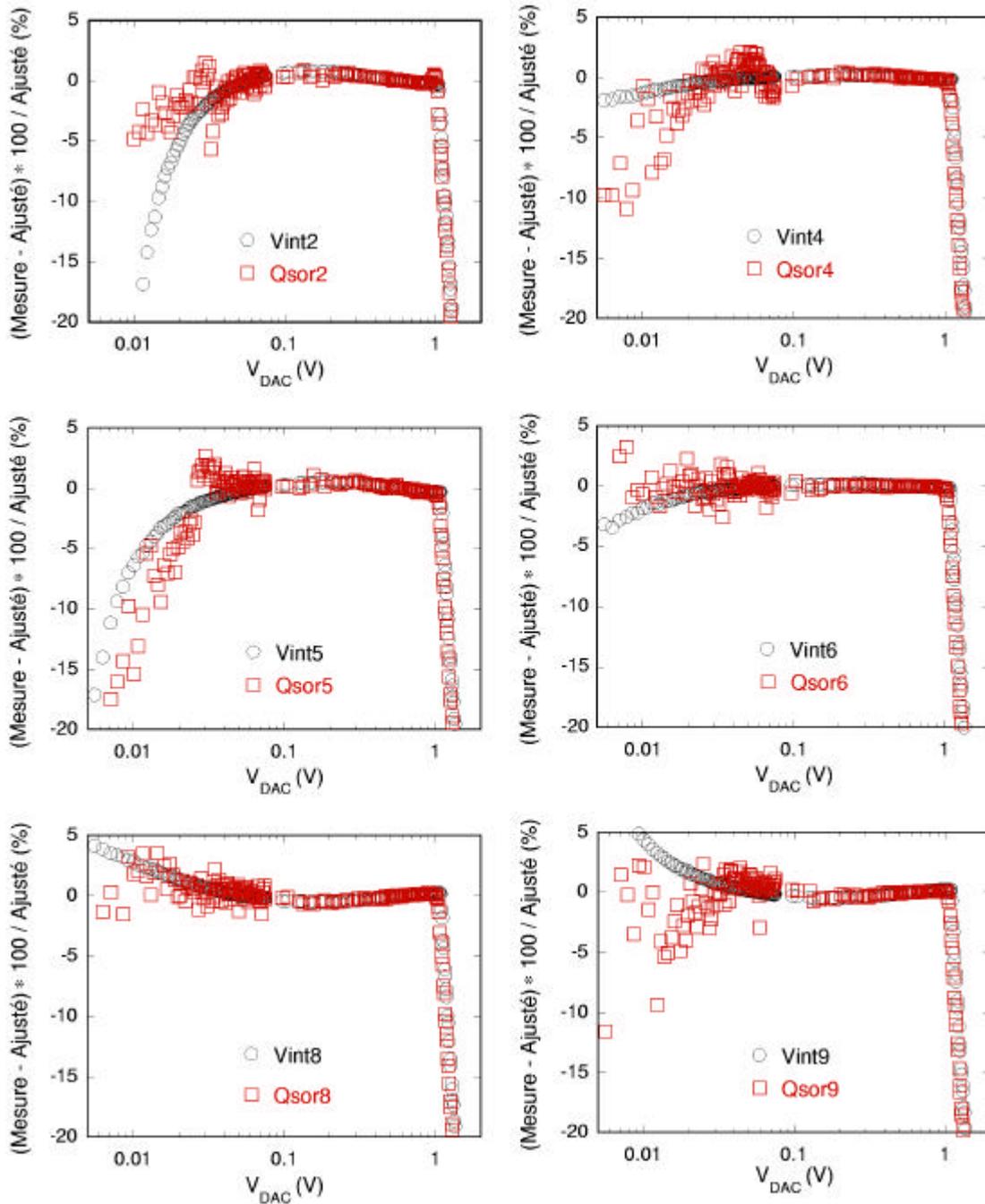


Figure 6: Pools of Q_{out} and V_{out} on linear fits, for six different DMILL bipolar injectors

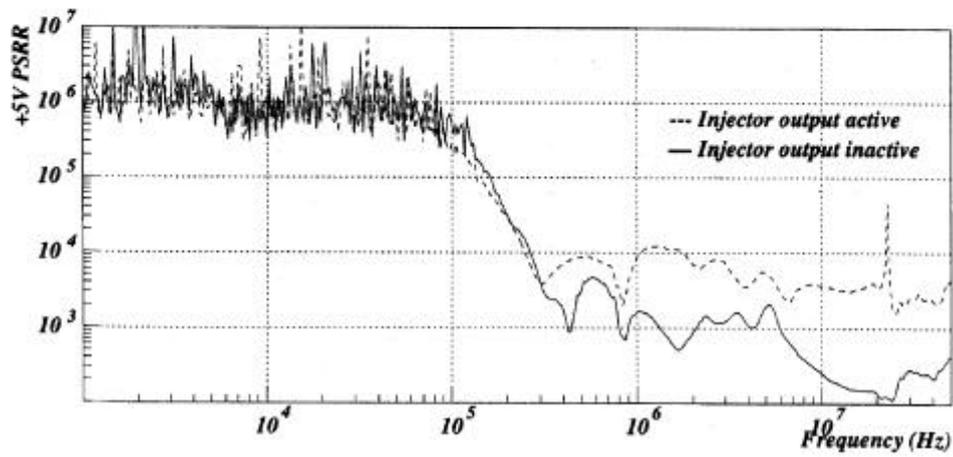
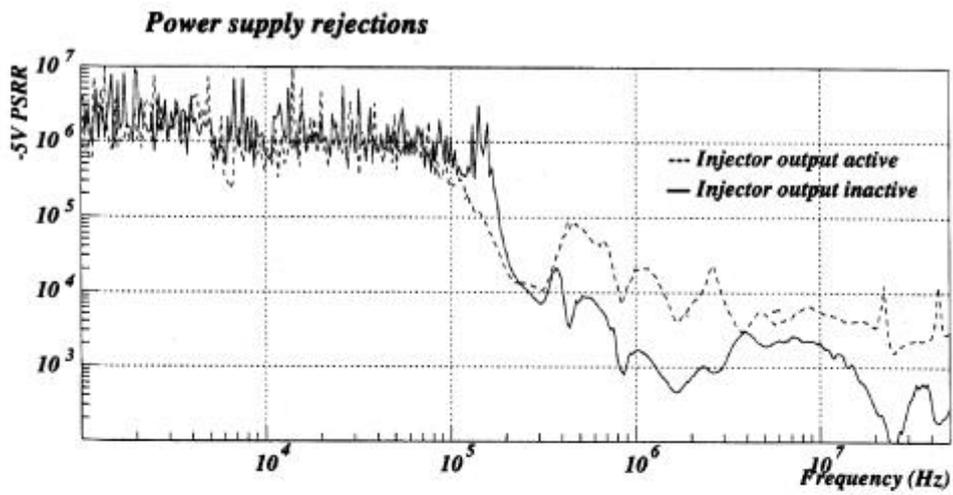


Figure 7: Power supply rejection ratios (PSRR) on the -5 V (top) and $+5\text{ V}$ (bottom) lines of a DMILL BiCMOS injector

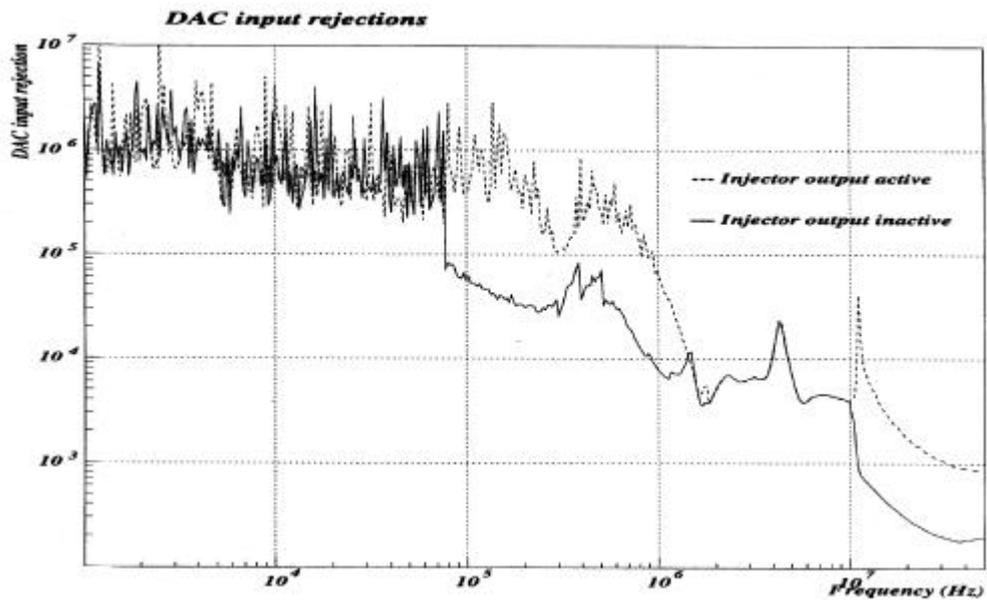


Figure 8: PSRR on the DAC line of a DMILL BiCMOS injector

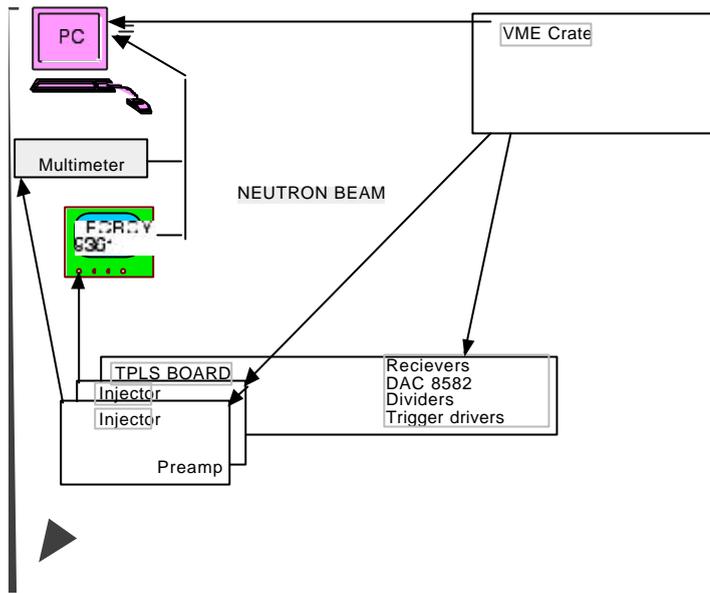


Figure 9: Set up for measurements on neutron beam

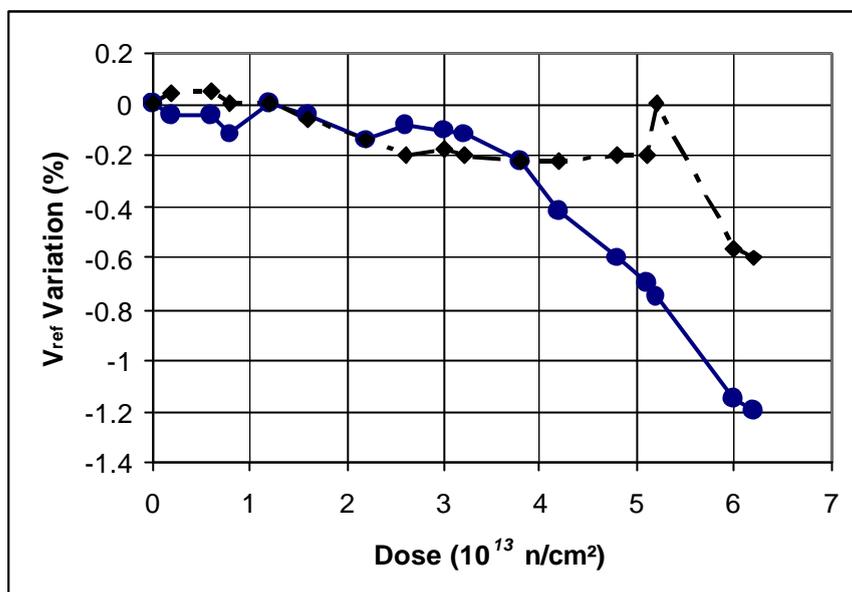


Figure 10: Drift of the V_{ref} for two DACs under neutron irradiation

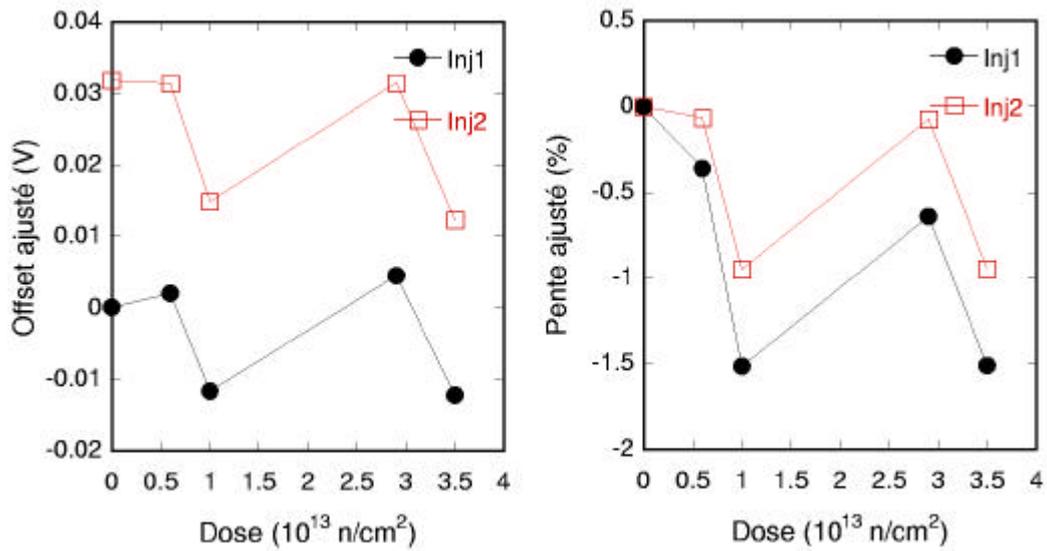


Figure 11: Examples of variations of the fitted offset and slope under irradiation

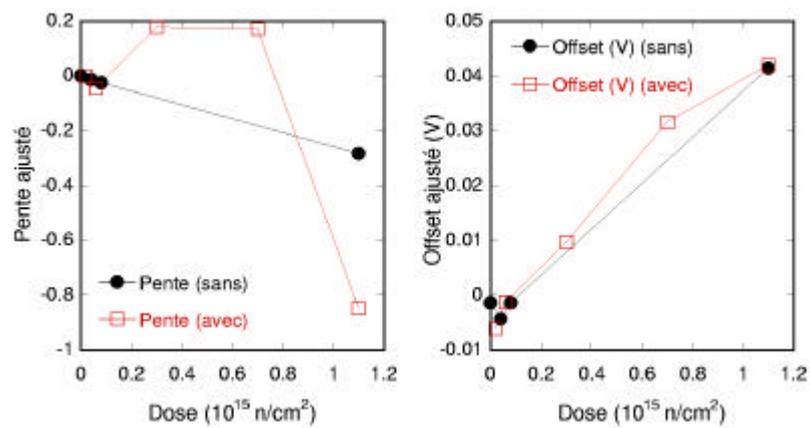


Figure 12: Shift of the slope (left) and offset (right) for extreme irradiation

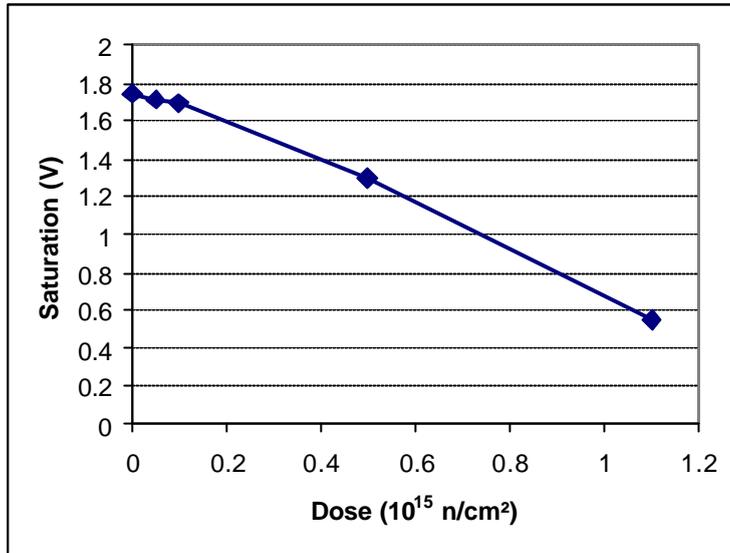


Figure 13: Variation of saturation for extreme irradiation

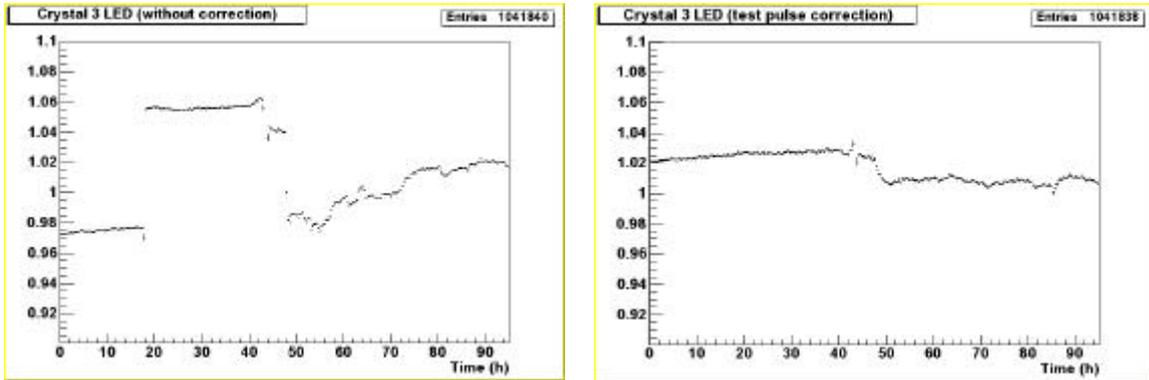


Figure 14: Example of signal correction by electronic Test Pulse calibration. On the Left side the signal is shown with no correction. On the right side the TP correction is applied.

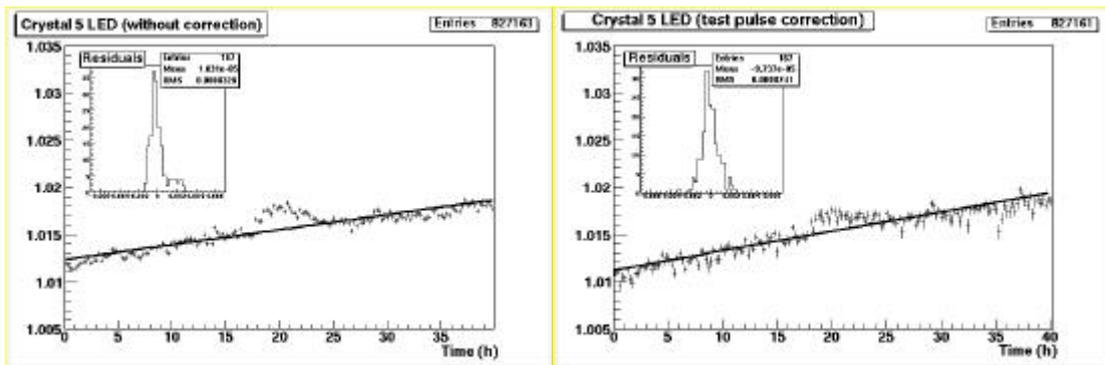


Figure 15: Example of correction applied on a LED signal. On the left side the LED signal is not corrected by the TP, while the TP correction is applied on the right side. The signal is not deteriorated by corrections.